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09/720,132	12/19/2000	Jacques Meyer	859063.464	8866

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EXAMINER	
WARE, CICELY Q	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/720,132	MEYER, JACQUES	
	Examiner	Art Unit	
	Cicely Ware	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 14-17* is/are rejected.

7)☒ Claim(s) *11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in France on 02/26/1999. It is noted, however, that applicant has not filed a certified copy of the foreign application as required by 35 U.S.C. 119(b).

2. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification of in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)). The specific reference to any prior nonprovisional application must include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

Specification

3. The abstract of the disclosure is objected to because:

   a. Examiner suggests applicant delete line 33.

   b. Line 20, examiner suggest applicant re-write this line for clarification, paying special attention to a reference (P).

Correction is required. See MPEP § 608.01(b).

4. The specification is objected to because applicant failed to place appropriate headings for sections of the disclosure. Examiner suggests applicant see 37 CFR 1.77

5. The disclosure is objected to because of the following informalities:

a. Pg. 2, line 12, applicant uses the phrase "in a window W of same length". Examiner suggests using "in a window W of the same length" for clarification purposes. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Klank et al. (US Patent 6,226,337).

(1) With regard to claim 1, Klank et al. discloses an OFDM demodulator comprising a fast Fourier transform circuit for analyzing a received signal in a window corresponding to one symbol, each symbol carrying several phase and amplitude modulated carriers, some of which, shifted in frequency in a predetermined way from one symbol to the next one, form pilots (col. 1, lines 32-38, col. 6, lines 56-63, col. 9, lines 52-67, col. 10, lines 1-6, 30-32, col. 11, lines 56-61, col. 14, lines 30-51); a bi-dimensional filter for interpolating, from anchors corresponding to the pilots such as received from several consecutive symbols, the distortion undergone by each carrier (col. 7, lines 55-59, col. 11, lines 62-67, col. 12, lines 6-12, 33-67); means for correcting window shifting with respect to an optimal position (col. 10, lines 47-65, col. 11, lines 1-3, 22-47); and means for correcting each distortion according to window shifting

corrections performed respectively for the symbol associated with the distortion and for the symbols associated with the anchors used to interpolate the distortion (col. 11,lines 4-47).

Klank et al. does not explicitly disclose an FFT. However it is well known in the art that a DFT algorithm is most easily executed using an FFT algorithm.

(2) With regard to claim 3, claim 3 inherits all the limitations of claim 1. Klank et al. further discloses wherein each distortion is, in the frequency field after Fourier transform, a weighted sum of two anchors of the same position in a preceding symbol and in a following symbol, to which anchors have been added respective phases corresponding to the shiftings undergone by the analysis window for the preceding and following symbols, and to which anchors has been subtracted a phase corresponding to the shifting undergone by the analysis window for the symbol associated with the distortion (col. 7, lines 17-19, col. 9, lines 63-67, col. 10, lines 44-65, col. 12, lines 13-32, 40-64, col. 13, lines 8-13).

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klank et al. (US Patent 6,226,337) as applied to claim 1 above, in view of Ikeda et al. (US Patent 5,506,836).

With regard to claim 2, claim 2 inherits all the limitations of claim 1. However Klank et al. does not disclose wherein the means for correcting the window shifting comprise a phase-locked loop synchronized on a correlation signal obtained by a correlation product between the received signal and this same signal delayed by one

symbol each symbol being preceded by a guard interval corresponding to a copy of the end of the symbol.

However Ikeda et al. discloses an OFDM demodulation apparatus (Fig. 5, (890), Fig. 3 (853, 854, 856, 869, 868)) means for correcting the window shifting comprise a phase-locked loop synchronized on a correlation signal obtained by a correlation product between the received signal and this same signal delayed by one symbol each symbol being preceded by a guard interval corresponding to a copy of the end of the symbol (col. 7, lines 66-67, col. 8, lines 1-55, col. 13, lines 5-15, 53-57, 63-67, col. 14, lines 1-5).

Therefore it would have been obvious to one of ordinary skill in the art to modify the invention of Klank et al. to incorporate means for correcting the window shifting, wherein the means comprise a phase-locked loop synchronized on a correlation signal obtained by a correlation product between the received signal and this same signal delayed by one symbol each symbol being preceded by a guard interval corresponding to a copy of the end of the symbol in order to correctly reproduce the carrier wave signals and clock signal and to correctly generate the DFT(FFT) time window.

9. Claims 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klank et al. (US Patent 6,226,337) in view of Ikeda et al. (US Patent 5,506,836).

(1) With regard to claim 4, Klank et al. discloses an OFDM demodulator with fast Fourier transform (FFT) analysis window displacement compensation, comprising: a reconstruction circuit configured to receive radio-transmitted signals in a window

corresponding to one symbol, the symbol carrying a plurality phase and amplitude modulated carriers, one or more of the carriers are shifted in frequency in a predetermined way from one symbol to the next symbol and form pilots, the reconstruction circuit configured to extract the symbols and convert the symbols into digital signals (col. 1, lines 5-8, col. 6,lines 17-19, col. 7, lines 51-67, col. 8, lines 1-7); an FFT circuit configured to perform a fast Fourier transform with the windows and output a transformed signal including complex coefficients (col. 3, lines 22-35). However Klank et al. does not disclose an adjustment circuit and an associated phase-locked loop (PLL) circuit configured to receive the digital signals and determine and readjust the position of the corresponding windows; a conversion circuit configured to receive a position signal from the PLL and to output a conversion signal that is corrected for distortion; a distortion interpolation circuit configured to receive the transformed signal and the conversion signal and to provide an interpolated distortion signal; and a correction circuit configured to receive the interpolated distortion signal and to output a corrected complex coefficients signal.

However Ikeda et al. discloses in (Fig. 3 (869), Fig. 5) an adjustment circuit and an associated phase-locked loop (PLL) circuit configured to receive the digital signals and determine and readjust the position of the corresponding windows (col. 13, lines 30-32, col. 14, lines 35-67, col. 15, lines 1-27); a conversion circuit configured to receive a position signal from the PLL and to output a conversion signal that is corrected for distortion (Fig. 3 (868), col. 13, lines 38-46, 63-67, col. 14, lines 1-5); a distortion interpolation circuit configured to receive the transformed signal and the conversion

signal and to provide an interpolated distortion signal (Fig. 3 (863, 864, 865, 868), col. 13, lines 38-46, 63-67, col. 14, lines 1-5); and a correction circuit configured to receive the interpolated distortion signal and to output a corrected complex coefficients signal (Fig. 3 (868)).

Therefore it would have been obvious to one of ordinary skill in the art to modify Klank et al. to incorporate an adjustment circuit and an associated phase-locked loop (PLL) circuit configured to receive the digital signals and determine and readjust the position of the corresponding windows; a conversion circuit configured to receive a position signal from the PLL and to output a conversion signal that is corrected for distortion; a distortion interpolation circuit configured to receive the transformed signal and the conversion signal and to provide an interpolated distortion signal; and a correction circuit configured to receive the interpolated distortion signal and to output a corrected complex coefficients signal in order to enable stable reproduction of a clock signal and as a result enable accurate demodulation with the stable operation of the PLL circuit and the DFT(FFT) circuit (Ikeda et al., col. 2, lines 62-63, col. 3, lines 4-6).

(2) With regard to claim 5, claim 5 inherits all the limitations of claim 4. Klank et al. further discloses in (Fig. 8, Fig. 9) a delay circuit coupled between the FFT circuit and the correction circuit and coupled in parallel with the distortion interpolation circuit (col. 10, lines 12-18, col. 12, lines 40-64).

(3) With regard to claim 6, claim 6 inherits all the limitations of claim 4. Ikeda et al. further discloses an OFDM demodulation apparatus (Fig. 5, (890), Fig. 3 (853, 854, 856, 869, 868)) means for correcting the window shifting comprise a phase-locked loop

synchronized on a correlation signal obtained by a correlation product between the received signal and this same signal delayed by one symbol each symbol being preceded by a guard interval corresponding to a copy of the end of the symbol (col. 7, lines 66-67, col. 8, lines 1-55, col. 13, lines 5-15, 53-57, 63-67, col. 14, lines 1-5).

(4) With regard to claim 7, claim 7 inherits all the limitations of claim 4. Ikeda et al. further discloses in (Fig. 5 (890, 895)) wherein the PLL comprises an accumulator that outputs the absolute position of the window with respect to a corresponding symbol.

(5) With regard to claim 8, claim 8 inherits all the limitations of claim 7. Ikeda et at. further discloses in (Fig. 5 (880, 890)) wherein the conversion circuit is configured to convert the absolute position received from the PLL into a form that is usable by the distortion interpolation circuit (Fig. 3 (863, 864, 865, 868), col. 13, lines 21-67, col. 14, lines 1-5, 23-67, col. 15, lines 1-27).

(6) With regard to claim 9, claim 9 inherits all the limitations of claim 4. Ikeda et al. further discloses wherein the PLL is configured to control the adjustment circuit col. 14, lines 1-5).

10. Claims 14 -17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klank et al. (US Patent 6,226,337) in view of Ikeda et al. (US Patent 5,506,836).

(1) With regard to claim 14, Klank et al. further discloses a method of fast Fourier transform (FFT) analysis window displacement compensation in a COFDM modulator, comprising: receiving a radio-transmitted signal in a window corresponding to one symbol, the symbol carrying a plurality of phase and amplitude modulated

carriers, one or more of the carriers are shifted in frequency in a predetermined way from one symbol to the next symbol and form pilots, and extracting the symbols and converting these symbols into digital signals (col. 1, lines 5-8, col. 6,lines 17-19, col. 7, lines 51-67, col. 8, lines 1-7); receiving the windows and performing a fast Fourier transform with the windows and outputting a transformed signal that includes complex coefficients (col. 3, lines 22-35). However Klank et al. does not disclose receiving the digital signals and determining and readjusting the position of the windows; receiving a position signal outputting a conversion signal that is corrected for distortion; receiving the transformed signal and the conversion signal and to providing an interpolated distortion signal; and receiving the interpolated signal and outputting a corrected complex coefficients signal.

However Ikeda et al. further discloses receiving the digital signals and determining and readjusting the position of the windows (col. 13, lines 30-32, col. 14, lines 35-67, col. 15, lines 1-27); receiving a position signal outputting a conversion signal that is corrected for distortion (Fig. 3 (868), col. 13, lines 38-46, 63-67, col. 14, lines 1-5); receiving the transformed signal and the conversion signal and to providing an interpolated distortion signal (Fig. 3 (863, 864, 865, 868), col. 13, lines 38-46, 63-67, col. 14, lines 1-5); and receiving the interpolated signal and outputting a corrected complex coefficients signal (Fig. 3 (868)).

Therefore it would have been obvious to one ordinary skill in the art to modify Klank et al. to incorporate receiving the digital signals and determining and readjusting the position of the windows; receiving a position signal outputting a conversion signal

that is corrected for distortion; receiving the transformed signal and the conversion signal and to providing an interpolated distortion signal; and receiving the interpolated signal and outputting a corrected complex coefficients signal in order to enable stable reproduction of a clock signal and as a result enable accurate demodulation with the stable operation of the PLL circuit and the DFT(FFT) circuit (Ikeda et al., col. 2, lines 62-63, col. 3, lines 4-6).

(2) With regard to claim 15, claim 15 inherits all the limitations of claim 14. Klank et al. further discloses in (Fig. 8 (DSE), Fig. 9 (FFT, FFTW, COR)) the method comprising receiving the transformed signal and outputting a delayed transformed signal.

(3) With regard to claim 16, claim 16 inherits all the limitations of claim 14. Ikeda et al. further discloses the method further comprising generating a phase-locked loop synchronized on a correlation signal obtained by a correlation product between the received signal and this same signal delayed by one symbol each symbol being preceded by a guard interval corresponding to a copy of the end of the symbol (col. 7, lines 66-67, col. 8, lines 1-55, col. 13, lines 5-15, 53-57, 63-67, col. 14, lines 1-5).

(4) With regard to claim 17, claim 17 inherits all the limitations of claim 14. Ikeda et al further discloses the method comprising calculating distortion (col. 7, lines 25-53).

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klank et al. (US Patent 6,226,337) as applied to claim 1 above, in view of Ikeda et al. (US Patent

5,506,836) as applied to claim 4 above, and further in view of Le Floch (US Patent 4,638,349).

With regard to claim 10, Klank et al. in combination with Ikeda et al. disclose all the limitations of claim 4 above. However Klank et al. in combination with Ikeda et al. do not disclose the demodulator wherein the interpolation circuit comprises: first, second, and third anchor input registers coupled to a first multiplexer; fourth, fifth, and sixth anchor input registers coupled to a second multiplexer; and first and second multipliers each having inputs coupled respectively to the first and second multiplexers, and each further having an output coupled to a common adder.

However Le Floch discloses in (Fig. 1d, 2) a digitally demodulating circuit wherein the interpolation circuit comprises: first, second, and third anchor input registers coupled to a first multiplexer; fourth, fifth, and sixth anchor input registers coupled to a second multiplexer; and first and second multipliers each having inputs coupled respectively to the first and second multiplexers, and each further having an output coupled to a common adder (col. 4, lines 44).

Therefore it would have been obvious to one of ordinary skill in the art modify the inventions of Klank et al. in combination with Ikeda et al. to incorporate the interpolation circuit comprising: first, second, and third anchor input registers coupled to a first multiplexer; fourth, fifth, and sixth anchor input registers coupled to a second multiplexer; and first and second multipliers each having inputs coupled respectively to the first and second multiplexers, and each further having an output coupled to a

common adder in order to synchronize the rate of the reference signals and the rate of the modulated signals using simple algebraic expressions (Le Floch, col. 2, lines 55-61).

Allowable Subject Matter

12. Claims 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 703-305-8326. The examiner can normally be reached on Monday – Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cicely Ware

cqw
January 12, 2004

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
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